DSP and digital down conversion

Ing. Ivo VIŠČOR, Ing. Josef HALÁMEK, CSc.
Institute of Scientific Instruments, Academy of Sciences of the Czech Republic
Královopolská 147, 612 64 Brno, Czech Republic, ivovi@isibrno.cz

Abstract: The comparison of three single chip digital down converters, their parameters, features and critical sections are presented.

1. Introduction

The digital quadrature detection and filtering were introduced by Hewlett-Packard in 1978. Its advantages and problems were discussed in more papers, but the real applications were limited by technological possibilities. Now, more special DSP exist. They include a fully programmable single chip synthesizer, quadrature mixer, and low pass filter, and it seems that the technological limitation disappears. But this is not quite true. These IC do not differ too much, but in some applications the difference can be significant, and still some limitation exists, and so the proper choice of IC is important. The aim of this contribution is to compare the HSP50016 and HSP50214 from Harris Semiconductor, and AD6620 from Analog Devices that are the best IC in this area.

2. Architecture

The block scheme of these circuits is in Fig.1. The basic blocks are: local oscillator (LO), digital quadrature detector (DQD) and decimation filter (DF). The architecture and so the function of some blocks are different.

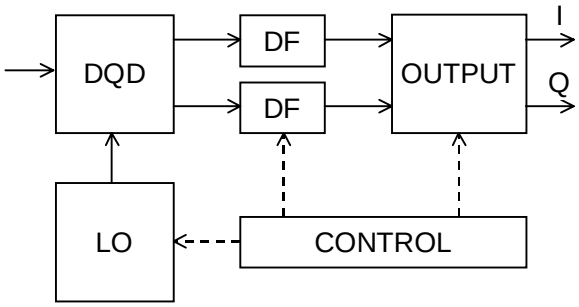

Fig.1. The digital down convertor architecture.

2.1 Local oscillator

The local oscillator produces a quadrature sinusoid with a programmable frequency and phase. The LO consists of a phase accumulator and sin/cos table. The phase register accumulates a phase increment every clock period. A part of the phase register word goes to the sin/cos table. There are three quantizations in the LO. The first quantization based on the width of the phase accumulator word determines a frequency step. The frequency step is $f_{CLK}/2^N$, where N is the width of the phase accumulator. The truncated phase, which goes to the sin/cos table, represents the second quantization. The quantization of the sin/cos amplitude is the third quantization. The second and third quatization are the source of the spurious at the output of LO. So the main parameters of LO can be expressed by the width of words and busses and are in Table 1. It is a pity that Analog Device uses only the spurious free dynamic range (SFDR) as a parameter. It is not so definite as the number of bits. SFDR depends not only on the number of bits, but also on the input noise and LO frequency. From Tab.1 we can see that this block is nearly equal for all IC, the small differences are in special functions of this block only.

LO parameters	HSP 50016	HSP 50214 A/B	AD 6620
Phase increment	32-bit	32-bit	32-bit
Phase accumulator	33-bit	32-bit	32-bit
Frequency step at $f_{S\,max}$	0,0088 Hz	0,0152 Hz	0,0152 Hz
Sin table argument	18-bit	18-bit	N/A
Sin table output	17-bit	18-bit	(SFDR = 100 dB)

Tab. 1.

2.2 Digital quadrature detector

The digital quadrature detector multiplies input real data and complex data from the LO. The parametrs of the DQD are: the width of words and maximal sampling frequency, Tab.2. The width of LO words and the DQD output determine the SFDR. The 14-bit width of input data of HSP50214 is not the limiting parameter, the contemporary fast ADC has no more than 14 bits.

DQD parameters	HSP 50016	HSP 50214 A/B	AD 6620
Input data	16-bit	14-bit	16-bit
$f_{S\,max}$	75 MHz	65 MHz	65 MHz
LO output data	17-bit	18-bit	(SFDR = 100 dB)
DQD output data	17-bit	15-bit	18-bit

Tab. 2.

2.3 Decimation filter

The decimation low pass filters are the most different block. They differ not only in parameters, but also in internal structure. The filter has always at least two steps; the first step makes the basic narrowing of the pass band and the corresponding sample decimation, the last is responsible for a good frequency response. The basic parameters are: the maximal pass band (limited by computing performance, output performance), minimal sample decimation, if the output frequency response is programmable or not, if the filter can be bypassed, and others. A simple comparison is difficult, we try to express it in Tab. 3.

DF parameters	HSP 50016	HSP 50214 A/B	AD 6620
Architecture	$COMB^5$ FIR	$COMB^5$ 5x HB FIR	$COMB^2$ $COMB^5$ FIR
Comb filter decimation	16 ÷ 32768	1; 4 ÷ 32	(1 ÷ 16) · (1 ÷ 32)
Halfband filters decimation	-	1 ÷ 32	-
FIR filter decimation	4	1 ÷ 16	1 ÷ 32
Overall decimation	64 ÷ 131072	1 ÷ 16384	1 ÷ 16384
Comb filter output	17-bit	24-bit	18-bit
Halfband filter output	-	24-bit	-
FIR filter output	38-bit	26-bit	23-bit
FIR filter length	121 taps	255 taps (max.)	256 taps (max.)
FIR coefficients	fixed	programmable	programmable
FIR coefficients resolution	22-bit	22-bit	20-bit
Max. pass band	645 kHz	2 037 kHz	1 300 kHz
Max. filter baypass output rate	disallowed	9,2 MSPS	32,5 MSPS
Max. dynamic range	110 dB	96 dB	120 dB

Tab. 3.

The first filter step is a comb filter. The comb filter has two parameters; the first is the decimation rate, which is programmable, and the second is the order of the comb filter, which

is fixed. The decimation and order determine the rejection of alias and so define the usable bandwidth for the desired rejection. In order to reduce power consumption of the comb stage, a low quality second order comb followed by a low clock fifth order comb is used for AD6620. The trade-off between the comb with a high decimation and FIR with a good response is a halfband filter. The halfband filter is a fixed response FIR with a decimation of 2 and 6 dB loss at the output Nyquist frequency. The HSP50214 uses a set of five halfband filters which have 7 (first) to 23 (last) taps.

With HSP50016 and AD6620 the maximal dynamic range is limited by the number of bits at the input of FIR filters and with HSP50214 by the width of the output word.

The differences in the main parameters of this block are significant and the choice of a proper IC goes out mostly from the maximal pass band, maximal and minimal decimation.

3. Output data and control

The output data can be parallel for a high throughput (not HSP5016) or serial for simple wiring. The data format possibilities are shown in Tab. 4. The output data I, Q of the HSP50016 can be taken either from two serial outputs (I, Q) or from one serial output I (I data followed by Q data). A multichannel operation using 64 words data frame may be set, but only the reset provides time slot synchronization. Each of two serial outputs of the HSP50214 can transmit up to 7 different data words (I, Q data and 5 other data types). The length of data word is 16 bits only and no multichannel operation is allowed. The AD6620 has only one serial output. It can use data frame signals to chain more DDC circuits into multichannel transfer.

The throughput of a serial port should be considered. For example, the HSP50016 demands 37 serial clocks to transmit 16-bit I, Q data through one serial port. This results in the 0,86 MSPS data rate with a 32 MHz serial clock. The HSP50214 needs 32 serial clocks (1 MSPS), and the AD6620 requires 48* serial clocks (0,67 MSPS) to transmit the same data.

It makes no sense to use more than 18 bits from the HSP50016 output and more than 20 bits from the AD6620 output regarding the maximal dynamic range of the IC. While the 16-bit output of the HSP50214 limits the output dynamic range, and a good 126 dB dynamic range at the FIR output is used only as a headroom for the on-chip AGC or as the input to the on-chip polar converter.

Output parameters	HSP 50016	HSP 50214 A/B	AD 6620
Output data	serial	serial and parallel	serial or parallel
Serial output data	16/24/32/38-bit	16-bit	16/24/32-bit
Serial output ports	2 or 1	2 or 1	1
Parallel o*utput ports	-	(2 or 1) x 16-bit	1 x 16-bit

Tab. 4.

All three IC must be initialized after reset through a control channel. The possibilities of control are in Table 5. Note that FIR coefficients must be transferred to HSP50214 and AD6620 after reset. After a parallel initialization, the AD6620 can also use serial control, even at the same time with the parallel one.

Control parameters	HSP 50016	HSP 50214 A/B	AD 6620
Serial control	yes	no	not for initialization
Parallel control	no	common 8-bit	common 8-bit
JTAG (IEE 1149.1)	yes	no	yes

Tab. 5.

* In case of the serial control, 32 clocks otherwise.

4. Special functions

Each of mentioned circuits offers some functions exceeding the basic DDC architecture. The HSP50016 offers a frequency sweeping of the LO and some spectral operations, the HSP50214 offers AGC, polyphase filter and cartesian to polar converter and the AD6620 offers processing of one complex or two real input signals. The main special functions are summarized in Table 6.

Special functions	HSP 50016	HSP 50214 A/B	AD 6620
Input data exponent	no	3-bit	3-bit
Input data zero-stuffing	no	yes	no
Input complex data	no	no	yes
Two input real data	no	no	yes
Input level detector	no	yes	no
LO dither option	no	no	argument, amplitude
LO frequency sweeping	sawtooth, triangle	no	no
Internal AGC loop	no	yes	no
Polyphase filter	no	yes	no
Interpolation filter	no	yes	no
Output real data	yes	no	no
Output spectral offset data	yes	no	no
Output polar data	no	yes	no
Frequency discriminator	no	yes	no
Output floating point data	32-bit	no	no
Multi-chip synchronization	no	yes	yes

Tab. 6.

Very useful is the LO frequency sweeping option of HSP50016. The LO can automatically produce frequency modulation by increasing or decreasing sawtooth or triangle. The HSP50214 cartesian to polar converter simplifies AM and PM demodulation. The on-chip frequency discriminator, which does subtraction of delayed phase samples, can execute FM demodulation. Another programmable 63-tap FIR can be exploited for postdetection filtration of the discriminator output (FM), magnitude output (AM) or I output (SSB). The LO dither option is interesting with AD6620. The argument and amplitude dither can be used together or alone. The dither improves the worst case SFDR from 100 dB to 118 dB at the cost of a slightly increased noise floor and rather spread carrier.

5. Conclusion

Some parameters and especially the special functions of IC suggest their applications. The HSP50214 with a polar converter, frequency discriminator and polyphase filter with a symbol tracking loop tends to general-purpose communication receivers (AM, SSB, PM, FM) and digital data receivers. The AD6620 with parallel acquisition of two signals considerably simplifies diversity receivers of GSM base stations. For general-purpose measurements and spectral analysis the HSP50016 and the HSP50214 can be used. The HSP50016 advantages are: sweeping option, maximal area of sample decimation, simple control and output. The disadvantage is the low pass band. The HSP50214 advantages are the maximal pass band, the digital filter bypass option, and the polar converter. In the control systems, HSP50016 is the best – maximal sample decimation, sweeping option.

References:

[1] Harris Semiconductor: Data sheet of HSP50016, 1996
[2] Harris Semiconductor: Data sheet of HSP50214A, 1998
[3] Analog Devices: Data sheet of AD6620, 1998