Clock signal requirement for high-frequency, high dynamic range acquisition systems

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(Received 28 June 2005; accepted 4 October 2005; published online 9 November 2005)

Analog-to-digital converters (ADC's) are increasingly replacing mixers in frequency conversion schemes. To achieve superior performances, in terms of bandwidth and dynamic range, a nearly ideal ADC clock is needed, with a spectral purity higher than the reference signal of the classical mixing scheme. These requirements of spectral purity for the ADC clock are discussed by analyzing in detail the nonuniform sampling process and by characterizing an actual acquisition system. The effect of clock phase imperfections on the output is proportional to the input frequency over sampling frequency ratio. Moreover, at the output we may have a multiple folding of the phase jitter spectrum. These effects are illustrated by three sets of measurements performed using our system: transfer of spurious clock components, aliasing of these components, and transfer of clock phase noise. © *2005 American Institute of Physics.* [DOI: 10.1063/1.2130937]

I. INTRODUCTION

Modern receivers often replace traditional IF mixing stages with high-speed sampling analog-to-digital converters (ADC's) of high dynamic range, and perform frequency conversion either by digital signal processing or by undersampling.

New sources of error signals emerge in this case, in particular ADC's static and dynamic nonlinearity and the nonregularity of the sampling intervals. Both these sources may be analyzed independently since cross terms are usually negligible. In this article, we address the nonregularity of the sampling intervals by means of analyzing an ideal ADC model driven by an imperfect clock signal.

The purity of the mixer reference signal is a well known issue of traditional frequency conversion. The output spectrum of an ideal mixer is the convolution between spectra of input and reference signals; any distortion in the reference signal is essentially transferred to the output. In direct IF or RF sampling schemes, the high-frequency clock signal plays roughly the role of the mixer reference signal. However, the relationship between nonidealities of clock signal and output is somewhat complicated, and there is more involved than just a spectral convolution. Consequently, to achieve the same performances with ideal ADC's and mixers, the purity requirements of the clock signal are significantly higher than those of the reference signal.

A further point, and one that has been mostly neglected in previous analyses of IF conversion by direct sampling, is the power-line interference, with first harmonics at 50 or 60 Hz. Such neglect would appear to be reasonable, since our signals belong to much higher frequency bands. However, when the final output of the receiver is a narrowband signal (several kHz) with a high dynamic range (>100 dB), the power-line interference may contribute significantly to the error budget of background noise of clock signal and noise components in proximity of clock frequency. In this article, we will compare the results obtained with analog mixers and AD converters in the presence of power-line interference.

II. METHOD

A. Sampling with jitter

The requirements of clock purity are usually expressed in terms of the time $\tau_{j\mathrm{rms}}$. With an ideal ADC and a noiseless harmonic signal of frequency f_{in} as the input, the signal-to-noise ratio of the output is given (in dB) by[1–4]

$$\mathrm{SNR}_j = -20\log(2\pi f_{\mathrm{in}}\tau_{j\mathrm{rms}}). \quad (1)$$

Here, $\tau_{j\mathrm{rms}}$ is the standard deviation of the sample instant in time. This equation is derived from the rms value of an error voltage, which is the product of the input signal slew-rate rms and the clock signal time jitter rms. Time jitter is assumed to have a white spectrum. However, Eq. (1) is valid for any type of jitter. Since this equation contains no information about the spectral distribution of output noise, it is of no help in identifying the bottlenecks of a system, or in suggesting an appropriate optimization. When using Eq. (1), it is necessary to evaluate $\tau_{j\mathrm{rms}}$ for the clock signal; this is usually done[2,3] by integrating the single-sideband power density of the phase noise. The simplest explanation of the different requirements of purity for an ADC clock and reference signal of a mixer will be given through an analysis of distortions associated with the small harmonic side band. This may arise as a product of the clock (or reference) signal with low-frequency interference.

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B. Effects of a spurious harmonic component in the clock (reference) signal

We have assumed an ideal harmonic input signal s_1 and a clock (or reference) signal s_0 corrupted by a spurious harmonic component of amplitude C:

$$s_1(t) = A \cos \omega_1 t,$$

$$s_0(t) = B \cos \omega_0 t + C \cos \omega_D t. \tag{2}$$

In an ideal sampling scheme, each sample is taken when the clock signal s_0 crosses zero in the positive direction. We have assumed that the spurious component is small: $C \ll B$, and hence it causes only a small variation of clock period, $|\tau_j| \ll T_0$. When also $|\tau_j| \ll T_1$, the error signal at the output may be written as the product of τ_j with the time derivative $s_1'(t)$ of the input. Neglecting the natural images due to sampling, the output signal $s_2(t)$ of the ADC is

$$s_2(t) \approx s_1(t) + s_1'1(t) \times \tau_j(t). \tag{3}$$

With a small spurious signal, the jitter is given approximately by the spurious signal divided by the time derivative of the ideal clock signal at its zero-crossing point,[5] $t_{zc} = nT_0 - T_0/4$:

$$\tau_j(t) \approx \frac{C \cos \omega_D t}{s_0'(t_{zc})} \approx \frac{C \cos \omega_D t}{B \omega_0}. \tag{4}$$

By combining Eqs. (3) and (4), the ADC output signal in the presence of a harmonic jitter is

$$s_2(t) \approx A \cos \omega_1 t - \frac{AC}{2B} \frac{\omega_1}{\omega_0} [\sin(\omega_1 + \omega_D)t + \sin(\omega_1 - \omega_D)t]. \tag{5}$$

A spurious signal at the clock input of relative amplitude C/B produces two spurious signals of relative amplitude $C\omega_1/2B\omega_0$ at the ADC output. Notice that in the mixing scheme, the spurious term amplitude in the output signal, $s_{2\mathrm{mix}}$, does not depend on the input and reference frequencies ω_1, ω_0:

$$s_{2\mathrm{mix}}(t) = s_1(t) \times s_0(t) = \frac{AB}{2} [\cos(\omega_1 + \omega_0)t + \cos(\omega_1 - \omega_0)t] + \frac{AC}{2} [\cos(\omega_1 + \omega_D)t + \cos(\omega_1 - \omega_D)t]. \tag{6}$$

In other words, the relative amplitude of spurious terms at the mixer output is equal to C/B, as in the input reference. In contrast, the spurious output of the ADC is the spurious component of the clock multiplied by a factor equal to the ratio between the signal frequency and the sampling frequency. A graphic illustration of the differences between sampling and mixing is given in Fig. 1.

It should be noted that the carrier with a single spurious signal can be split into two modulated signals: amplitude and phase. As can be seen in the mixer of Fig. 1(a), both AM and PM components are transferred from the reference signal.

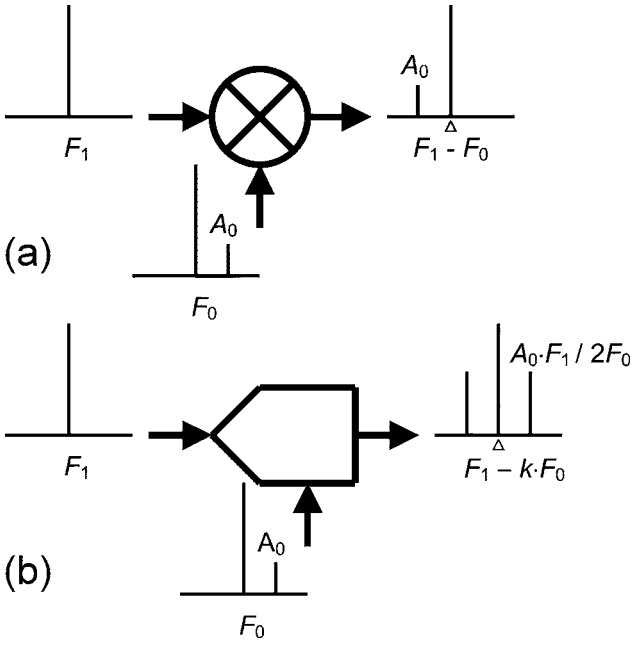

FIG. 1. Sensitivity of mixer (a) and ADC (b) to a spurious harmonic signal in the reference or clock signal: F_0= frequency of reference/clock; F_1= frequency of input signal; A_0 [=(C/B)] is the relative amplitude of the spur. The figure corresponds to the case of (a) $F_1 > F_0$ and (b) $kF_0 < F_1(k+0.5)F_0$, k=0, 1, 2,… .

In an ideal ADC, only the phase-modulation components are transferred from the clock signal, and in addition, they are multiplied by the ratio input frequency over clock frequency.

C. Uniform and nonuniform sampling

We shall now discuss the sampling process in detail in order to understand how distortions of various types affect the output signal. The following description is inspired by a model[6] of a nonuniformly sampling digital-to-analog converter. We begin with an ideally sampled output, s_{2i}, with a sampling period of T_0:

$$s_{2i}(t) = \sum_{n=-\infty}^{\infty} s_1(t) \times \delta(t - nT_0). \tag{7}$$

The spectrum of this signal is the convolution of the input signal spectrum with the spectrum of a train of delta functions,

$$S_{2i}(\omega) = \frac{1}{T_0} \sum_{k=-\infty}^{\infty} S_1(\omega - k\omega_0). \tag{8}$$

With a jittered clock signal, we have two possibilities:

(a) We can analyze the analog signal at the output of an ideal D/A converter which restores an analog signal by using the same clock used by the ADC. In this case,[1,2] the output signal s_{2m} is again the result of a plain multiplication,

$$s_{2m}(t) = \sum_{n=-\infty}^{\infty} s_1(t) \times \delta[t - nT_0 - \tau_j(t)], \tag{9}$$

where τ_j is the time jitter of the clock. The spectrum is the

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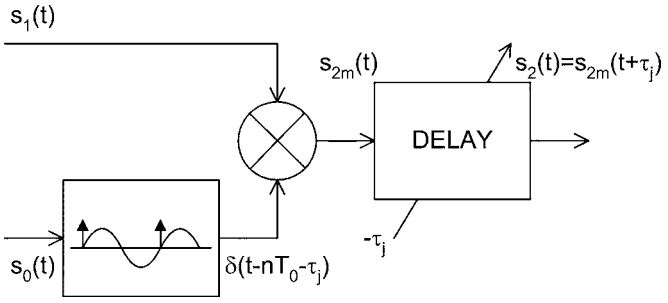

FIG. 2. Nonuniform sampling ADC model.

convolution of the input spectrum and the spectrum $S_{0m}(\omega)$ of the nonregular train of pulses,

$$S_{2m}(\omega) = \frac{1}{2\pi} S_1(\omega) \circ S_{0m}(\omega). \tag{10}$$

(b) Alternatively in a real system, the samples are assumed to have been acquired at regular intervals during the processing and analysis, or possibly the samples are restored to analog domain by a D/A converter with the ideal clock. The distortion of the clock embedded in the resulting signal is either amplified or attenuated depending upon the slew rate of the input signal. The resulting output signal s_2 may be written as

$$s_2(t) = \sum_{n=-\infty}^{\infty} s_1[t + \tau_j(t)] \times \delta(t - nT_0). \tag{11}$$

This description, represented in Fig. 2, reflects the real situation. This was therefore why the description (11) was taken in example B and will also be taken in the following analysis. The first block in Fig. 2, the clock-shaping circuit, generates pulses at the positive zero crossing of the clock signal. The input signal is multiplied by sampling pulses in the multiplier. The time alignment of the output samples is represented by a noncausal variable delay. The delay block can be placed at both the input and the clock signal without changing the output signal.

D. Harmonic signal sampled by a clock with phase modulation

We have assumed a harmonic input signal, s_1, and a harmonic clock signal, s_0, corrupted by a phase modulation $\phi_0(t)$, which causes the time jitter $\tau_j(t) = \phi_0(t)/\omega_0$:

$$s_1(t) = \cos \omega_1 t,$$

$$s_0(t) = \cos[\omega_0 t + \phi_0(t)]. \tag{12}$$

It is convenient to write the input and output signals in the complex form. The complex input signal is $s_{1C}(t) = \exp(i\omega_1 t)$ while, according to (11), the complex output is

$$\begin{aligned} s_{2C}(t) &= \sum_{n=-\infty}^{\infty} \exp\{i\omega_1[t + \tau_j(t)]\} \times \delta(t - nT_0) \\ &= \exp(i\omega_1 t) \times \exp[i\omega_1 \tau_j(t)] \times \sum_{n=-\infty}^{\infty} \delta(t - nT_0) \\ &\equiv a(t) \times b(t) \times c(t). \end{aligned} \tag{13}$$

The spectrum of this signal can be written as the convolution of the spectra of parts a, b, and c:

$$\begin{aligned} S_{2C}(\omega) &= \frac{A(\omega) \circ B(\omega) \circ C(\omega)}{(2\pi)^2} \\ &= \frac{1}{T_0} \sum_{k=-\infty}^{\infty} B[\omega - (\omega_1 + k\omega_0)]. \end{aligned} \tag{14}$$

A real input signal may be written as $s_1(t) = 0.5 \exp(i\omega_1 t) + 0.5 \exp(-i\omega_1 t)$ and its spectrum is immediately obtained from Eq. (14),

$$\begin{aligned} S_2(\omega) = \frac{1}{2T_0} \sum_{k=-\infty}^{\infty} & B[\omega - (\omega_1 + k\omega_0)] \\ & + B[-\omega + (-\omega_1 - k\omega_0)]. \end{aligned} \tag{15}$$

The spectrum of the modified clock phase noise $B(\omega)$ is replicated with the period of the sampling frequency ω_0. This means that a wideband phase noise at the ADC clock input may be folded many times in the Nyquist band. When the phase noise $B(\omega)$ has no components outside the interval $\langle -\omega_2, \omega_0/2 - \omega_2 \rangle$, with $\omega_2 = \min|\omega_1 + k\omega_0|$, aliasing does not occur and the output spectrum is

$$S_{20}(\omega) = \frac{1}{2T_0}[B(\omega - \omega_2) + B(-\omega + \omega_2)]. \tag{16}$$

From this equation we finally retrieve the ADC output signal in the time

$$\begin{aligned} s_{20}(t) &= \frac{1}{2T_0}\{\exp[i\omega_2 t + i\omega_1 \tau_j(t)] \\ &\quad + \exp[-i\omega_2 t - i\omega_1 \tau_j(t)]\} \\ &= \frac{1}{2T_0}\{\exp[i\omega_2 t + i\omega_1 \phi_0(t)/\omega_0] \\ &\quad + \exp[-i\omega_2 t - i\omega_1 \phi_0(t)/\omega_0]\}. \end{aligned} \tag{17}$$

This equation formally demonstrates that the clock phase jitter $\phi_0(t)$ is found at the output multiplied by the factor "input frequency/clock frequency"

$$\phi_2(t) = \phi_0(t) \frac{\omega_1}{\omega_0}. \tag{18}$$

However, it is more convenient to retrieve an expression for the single-sideband noise density at the ADC output, which is a more useful quantity than the phase jitter. We will consider only a small phase jitter, such that $|\phi_2(t)| \ll 2\pi$. In this way, we can apply the $\sin x \approx x$ approximation and therefore the distortion factor in the output signal is written as

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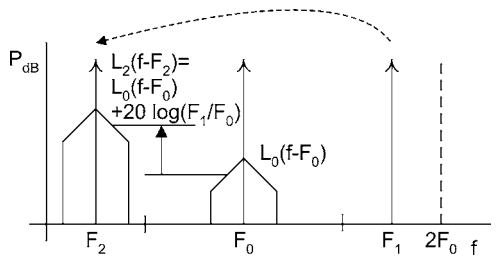

FIG. 3. Single-sideband phase noise amplification with an undersampling ADC. Input harmonic signal of frequency F_1 is sampled by clock signal of frequency F_0 with phase noise L_0.

$$b(t) = \exp[i\phi_2(t)] \approx 1 + i\phi_2(t). \tag{19}$$

The magnitude spectrum of $b(t)$ is symmetrical, $|B(\omega)| = |B(-\omega)|$, with a delta pulse at $\omega = 0$. The small jitter approximation Eq. (19) does not apply to the large accumulated[7] jitter $|\phi_2(t)| > 2\pi$ of a free-running clock oscillator, where the phase noise may be described[8] by the Wiener process. However, Eqs. (15)–(18) are also valid in this case.

Equation (19) implies that in the small phase jitter case, the relative power density $L_2(\omega)$ of the single-sideband phase noise is equal to the power spectrum of the phase jitter $\phi_2(t)$. The relationship between input and output noise spectra $S_\phi(\omega)$ and relative power densities is therefore

$$L_2(\omega) = |S_{\phi_2}(\omega)|^2 = \left| S_{\phi_0}(\omega)\frac{\omega_1}{\omega_0} \right|^2 = L_0(\omega) \times \left(\frac{\omega_1}{\omega_0}\right)^2. \tag{20}$$

The case of the ADC conversion is represented graphically in Fig. 3. The single-sideband phase-noise power at the output is the input noise power multiplied by the square of the frequency ratio $f_{\text{in}}/f_{\text{clock}}$. Conversely, in the case of the mixer, the output signal is given by

$$s_{2\text{mix}}(t) = s_1(t) \times s_0(t) = \cos[(\omega_1 + \omega_0)t + \phi_0(t)] + \cos[(\omega_1 - \omega_0)t - \phi_0(t)] \tag{21}$$

and the phase noise is transferred without amplification from input to output: $\phi_{2\text{mix}}(t) = \phi_0(t), L_{2\text{mix}}(\omega) = L_0(\omega)$.

E. General signal sampled by a clock with small phase modulation

We shall now take into consideration a generic, frequency-limited ($< \omega_{1\,\max}$) input signal $s_1(t)$ within the small phase-jitter approximation, which now reads $\phi_2(t) \leqslant \phi_0(t) \cdot \omega_{1\,\max}/\omega_0 \leqslant 2\pi$. By applying the approximation of Eq. (3), the error calculation is possible by means of the input signal derivation and the time jitter τ_j. Equation (11) can be rewritten for the output signal as

$$s_2(t) = \sum_{n=-\infty}^{\infty} s_1[t + \tau_j(t)] \times \delta(t - nT_0) = \left[s_1(t) + \frac{ds_1(t)}{dt}\frac{\phi_0(t)}{\omega_0} \right] \sum_{n=-\infty}^{\infty} \delta(t - nT_0). \tag{22}$$

The output spectrum S_2 is written as the convolution of the Fourier transformation of the factors in Eq. (22),

$$S_2(\omega) = \left\{ S_1(\omega) + \frac{1}{2\pi}\left[i\frac{\omega}{\omega_0} S_1(\omega) \right] \circ S_{\phi_0}(\omega) \right\} \circ \frac{1}{T_0} \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_0) = \frac{1}{T_0}\left(\sum_{k=-\infty}^{\infty} S_1(\omega - k\omega_0) + i\frac{1}{2\pi}\left[\frac{\omega}{\omega_0} S_1(\omega) \right] \circ \sum_{k=-\infty}^{\infty} S_{\phi_0}(\omega - k\omega_0) \right). \tag{23}$$

The clock phase noise spectrum is again aliased into the Nyquist band and, in addition, is now blurred by the high-frequency components of the input signal.

III. EXPERIMENTAL RESULTS

The measurements were taken using our digital receiver,[9] specifically designed for use in NMR and other biomedical applications, where a high dynamic range and a broad frequency range are required. The two-channel receiver is based on the 14-bit ADC AD6644 and the digital downconverter (DDC) AD6620, the latter of which performs digital conversion to baseband, filtering, and decimation of the sample rate. The decimated signal is then transferred to a computer for further processing.

A. Sample clock with spurs

As a clock, our converters may use either a simple onboard 66 MHz crystal oscillator or a signal from an external source. In an early version of the onboard oscillator, ripples of the power supply (about 0.1 mV) caused some frequency modulation, at a measured rate of 300 Hz/V. The resulting frequency deviation of $\Delta f \approx 30$ mHz induces 50 Hz parasitic sideband spurs. With a narrowband modulation ($f_m \approx 50$ Hz), the relative amplitude of these sidebands is half the modulation index $\Delta f/f_m \approx 0.0006$, which means these spurs in the clock signal are at about −70 dBc. With a 100 MHz input, these spurs are amplified by 4 dB in the output, and reduced by 16 dB with a 10 MHz input (see Fig. 4), exactly as predicted by Eq. (5).

B. Sample clock with phase noise

Three "pure" harmonic signals at 10 , 70, and 130 MHz were used as inputs. Their spectra, measured with our receiver together with a "pure" sample clock 66 MHz, are superimposed in Fig. 5(a). The noise floor of the 10 MHz signal is barely registered on the scale. To measure the influence of the clock phase noise upon the output sampled signal, we have added noise to the clock signal by means of a phase modulator and a noise generator. The spectrum of this clock signal has been determined by feeding it in our digital receiver as the input, using our "pure" clock at 66 MHz, see Fig. 5(b). The phase noise had a peak at 500 kHz offset, created by an artificial emphasis of the modulation noise in the filter in order to aid identification of the noise sideband effect. The small asymmetry between the lower and upper

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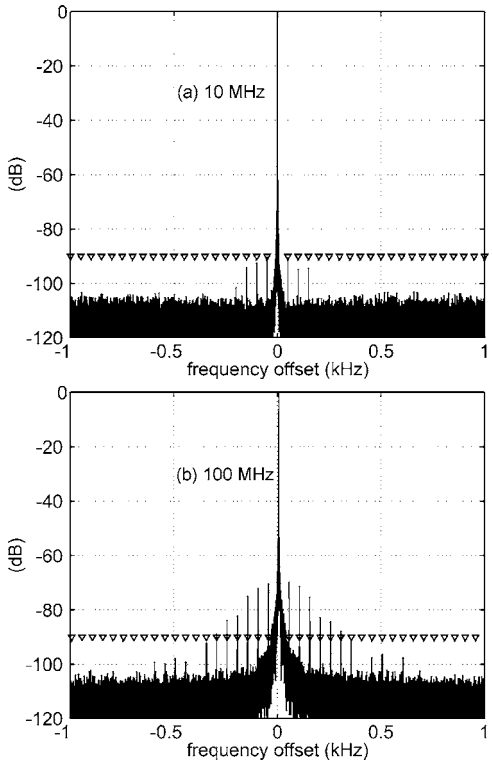

FIG. 4. Harmonic signals at (a) $f_1 = 10$ MHz and (b) $f_1 = 100$ MHz converted to a 2 kHz baseband by our digital receiver, which has a clock signal with spurs (see text). The "∇" markers are at 50 Hz intervals.

sideband of this noise is caused by an imperfect phase modulator, and by superposition of amplitude and phase modulations.

Figure 5(c) shows the spectra of the three input signals acquired using the noisy clock signal of Fig. 5(b). A comparison of the spectra of Figs. 5(b) and 5(c) demonstrates the phenomenon of phase-noise amplification by a factor equal to the input-to-sampling frequency ratio, as predicted by Eq. (20).

C. Bandwidth of the ADC clock input

The bandwidth of the clock input is a parameter never mentioned in the ADC datasheets. However, this bandwidth determines the possible folding of spurious tones and noise from the clock signal into the output, as predicted by Eq. (15). A test was done with a pure input signal of 89 MHz. The pure sample clock, at 15 MHz, was combined with a spurious −40 dBc signal whose frequency was varied from 5 to 500 MHz in 15 MHz steps. Analysis is made easy by the fact that the alias frequencies of the spurious components of the clock are always at 4 and 6 MHz. The amplitude of the output component caused by the spurious clock signal is shown in Fig. 6 for two conditions: with compensated (dashed line) and noncompensated clock transformer. The theoretical amplitude of the spurious signal at the output is −31 dBc. This result was obtained by the addition of 15 dB to the −40 dBc spurious level due to the input-to-clock frequency ratio (89/15), and the subtraction of 6 dB due to

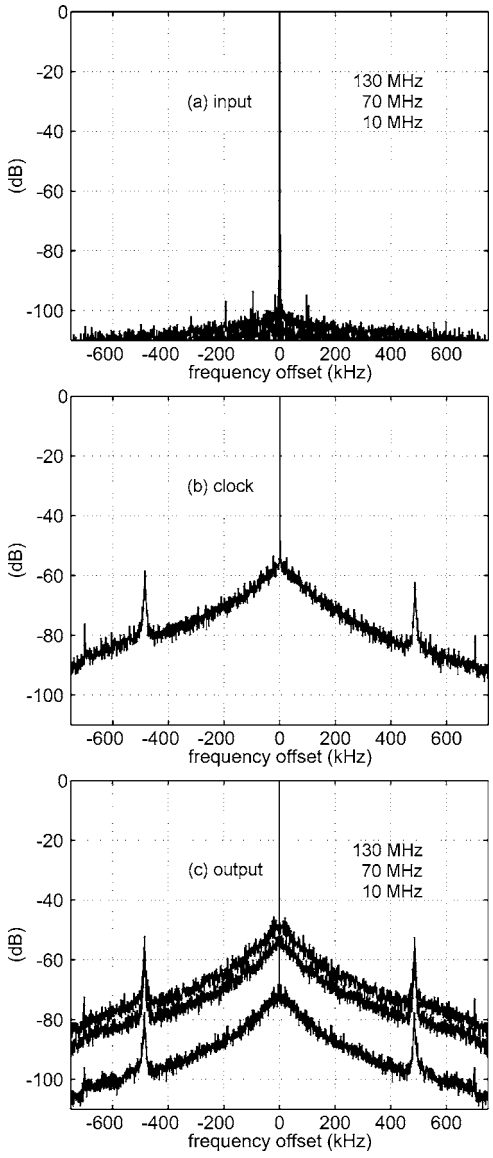

FIG. 5. (a) Harmonic signals at 10, 70, and 130 MHz measured by our digital receiver with a "pure" clock signal; (b) spectrum of a noisy clock signal at 60 MHz, obtained with our receiver and a "pure" clock signal; (c) harmonic signals of part (a) obtained when using the noisy clock signal (b). FFT 32k, bandwidth (fs_{out}) of 1.5 MHz.

the splitting into two phase-modulation sidebands. As one can see in Fig. 6, the 3 dB point of the clock input is about at 100 MHz.

IV. DISCUSSION

When using high dynamic range ADC systems for undersampling, the clock signal should be purer than the reference signal of a mixer of comparable performance. The distortions in the ADC output have a spectrum that results from convolution of the input signal spectrum and clock distortion spectrum multiplied by the input frequency over clock frequency ratio. Since the ADC's clock input is always broadband, frequency-distant noise and spurious components of the clock signal are potentially contributing to noise and distortions. On the other hand, only the phase distortion of a

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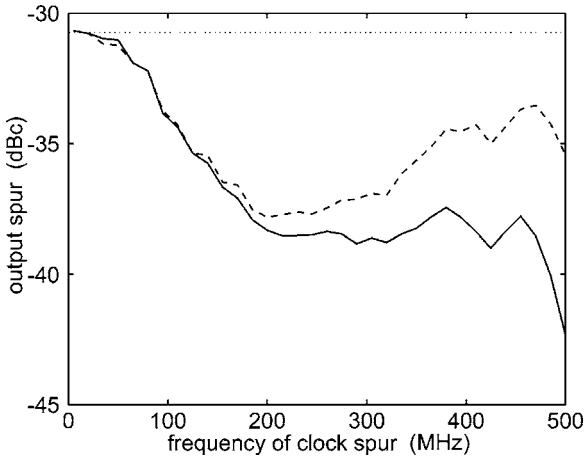

FIG. 6. Bandwidth of the AD6644 clock input determined from the output alias of spurious as follows: input signal of 89 MHz sampled at 15 MHz with addition to the clock of a −40 dBc signal at frequency ranging from 5 to 500 MHz. The dotted line is the theoretical amplitude; solid and dashed lines are data without and with compensation of a clock transformer, respectively.

clock signal plays a role in digital frequency converters, while both amplitude and phase distortions contribute to the output of mixers.

The clock inputs of ADC in broadband conversion schemes should undergo a strictly analog signal processing; no logic gates or amplifiers should be used in ADC clock distribution. If needed, the amplifiers should be followed by a bandpass filter to remove noise or spurs folded potentially into the Nyquist band due to the large bandwidth of the ADC clock input. In narrowband applications, a spurious-free-dynamic range of 100 dBc may be achieved with several of today ADC's. In this case, care must be taken to manage properly the power-line interference, which may otherwise couple by phase modulation to the clock input.

ACKNOWLEDGMENT

This work was supported by a grant of the Grant Agency of the Czech Republic No. 102/02/0553.

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