Two-channel digital receiver as a measurement unit

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Abstract: *A digital receiver was proposed. This paper discusses the critical hardware sections, the limiting system parameters and the first measurements.*

1. Introduction

The bandpass signal analysis is mostly based on quadrature detection and narrow-band filtration. The advantages of digital solution are: simplicity, high dynamic range and a strong rejection of the mixer image. The concurrent analysis of two signals is a frequent requirement. The two-channel digital receiver was proposed and realized as a receiver for NMR spectroscopy, the measurement of the analog-to-digital converter and for the experiments in communications. The key demands are: maximal dynamic range, high passband, parallel acquisition of two bands and the possibility to acquire the whole Nyquist band with no decimation.

2. The receiver architecture

The block schema of the receiver is shown in Fig.1. The basic blocks are: an optional sample-clock oscillator, an analog-to-digital converter (ADC), two single digital down converters (DDC) and a digital signal processor (DSP) unit. The ADC is the new one AD6644 (65 MSPS, 14-bit) acquired from Analog Devices as a paid preliminary sample. Three DDC chips were compared [1], the selected one is AD6620 (65 MSPS in, 1.3 MSPS out, 120 dB dynamic range). The DSP unit is a formerly completed and exploited plug-in board based on ADSP-2181 (1M words x 16 bit external memory).

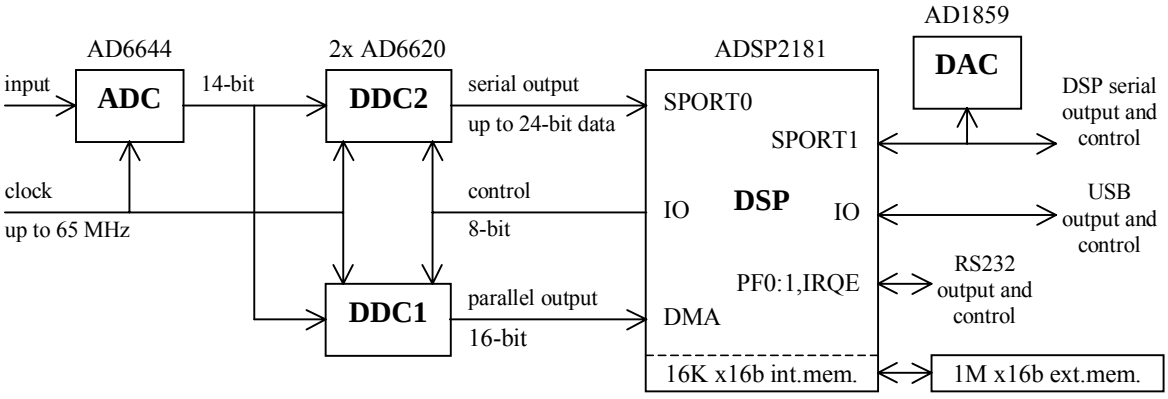

Fig.1. The two-channel digital receiver architecture

3. Hardware pitfalls

3.3V supply voltage of AD6620. The supply voltage of AD6620 differs from the 5V supply of DSP. This constrains the designer to assure level matching of 3.3V and 5V logic. The AD6620's outputs are 5V-TTL logic compatible, unlike the inputs which are not 5V-TTL tolerant. The proposed solution employs a glue-logic based on LCX product line produced by Fairchild and Motorola. (TI and Philips produce a similar LVC family.) This 3.3V logic has 5V tolerant inputs.

The ADC clock distribution. In order to minimize the system jitter, no active components are used for sample clock distribution. The clock signal from an onboard crystal oscillator or an external source is directly fed through a RF transformer to ADC.

The initial condition setting of AD6620. For NMR spectroscopy it is necessary to ensure a consistent reset of all signal and control registers (comb accumulators, FIR taps, phase accumulator) before the signal is fed in to preserve the phase coherency. The most secure solution is to feed in the zero signal of sufficient duration. This is accomplished by insertion of D-type flip-flops (74LCX574) between ADC and DDC with pull-down resistors. The zero-signal is produced when output enable (OE) pins of flip-flops are inactive.

The auxiliary clock generation for AD6620. The programming of AD6620 is just synchronous. The write of a control register takes 5 clock periods. Unfortunately, both the acquired signal and the clock signal are gated in the NMR spectroscope. It is necessary to generate an auxiliary clock signal so that the AD6620 can be programmed and zero-stuffed before the signal is fed in. The auxiliary clock is generated by the software at a DSP port.

The A/B signal generation for AD6620. In order to fulfil the requirement of data transfer from ADC through AD6620 to DSP without processing in AD6620, it is necessary to collect one output sample per one input sample. However, this is impossible when the real input mode of AD6620 is used (real input, complex multiplexed output). The solution is the utilising of the complex input mode of AD6620. The real input samples are acquired as complex multiplexed data. The odd samples are considered as real parts and even samples as imaginary parts of the input complex data. This allows to pass through just one sample per clock period. The A/B signal controlling the multiplex is generated by a simple flip-flop, which changes the state every clock period.

The programming of AD6620. The write of a control register takes 5 clock periods of DDC. If the DSP clock is 33 MHz and the wait states maximum of an IO port is 7, the minimal frequency of AD6620 clock (and also ADC clock) have to be 23 MHz. If one wants to take advantage of dynamic control of AD6620 for a lower sampling rate, it is necessary to prolong data write. The proposed solution uses the two-way D-type flip-flops/transceivers 74LCX652. This enables to control AD6620 without restriction and even read-back data from AD6620.

The parallel data output from AD6620 utilising DMA. For the maximal data throughput the DMA is used. The DMA transfer carries the 16-bit samples from AD6620 to DSP with no software overhead. One DMA transfer takes about 120 ns in ADSP2181, which are 4 processor clock periods. However, the AD6620's control outputs enables to generate two successive write pulses (for real and imaginary parts), which are distant only 15 ns (65 MHz clock). Fortunately, the real sample (I) is available in the first clock period at the AD6620 output and the imaginary sample (Q) is available in all the remaining clock cycles of the decimation period. The proposed circuit employs the auxiliary D-type register collecting the sample from AD6620 and a pulse generator to properly write the captured data to DSP. The pulse generator creates the first pulse at the beginning and the second one in the middle of the decimation period. The programmable pulse delay is made of the 4-bit counter with preset (74AC161).

The serial data output from AD6620. Unlike the parallel one the AD6620's serial output is simple and can transfer 24-bit samples, however the throughput is lower. The problem arises from the fact that AD6620's serial output is framed with the frame length related to the decimation rate unlike the ADSP2181 which can receive only the 24- or 32-word frames (multichannel mode). There is no problem if the decimation is greater than or equal to 768, because the transfer of one I-Q pair fits into one 24-word frame of DSP. When more than one I-Q pair transfer per 24-word frame arises, appropriate attention should be paid to the DSP serial port programming. Not all decimation rates can be used.

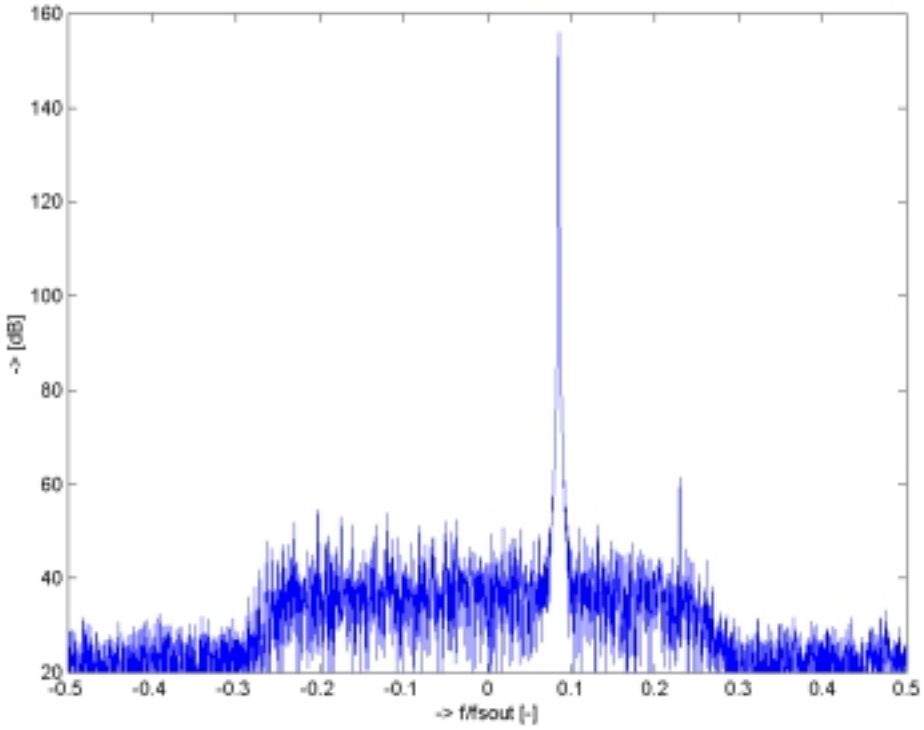

Fig. 2. Spectra of the full scale signal with a frequency of 2.24 MHz (generator HP 33120A). Sampling frequency 60 MHz, mixing frequency 2.20 MHz, output sampling frequency 469 kHz, data size 4 K (complex), Hanning window.

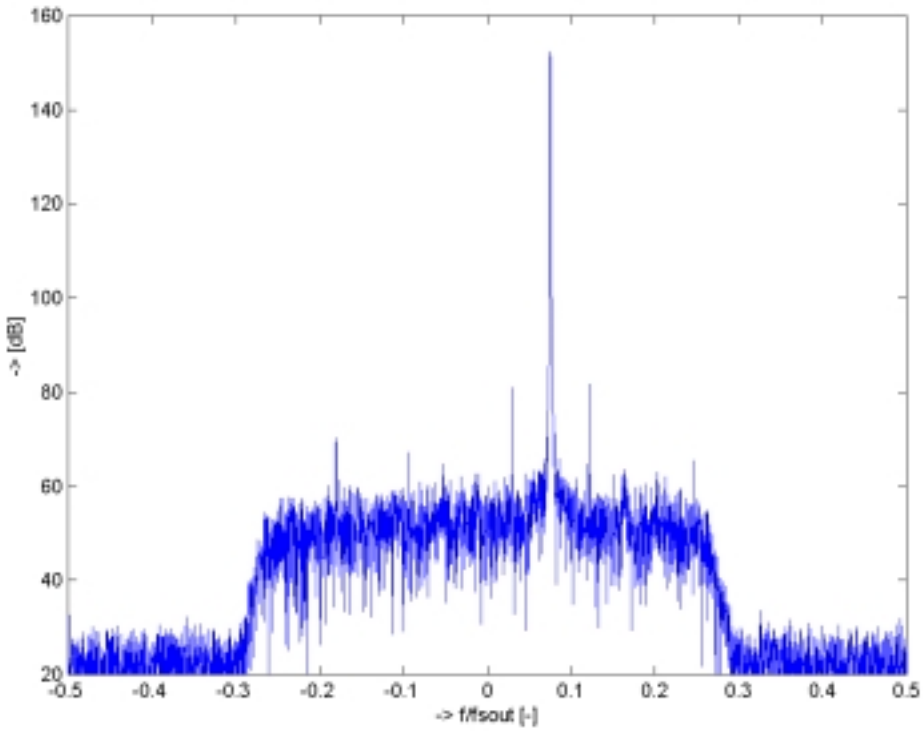

Fig. 3. Spectra of the full scale signal with a frequency of 362.24 MHz (synthesizer PTS 500). Sampling frequency 60 MHz, mixing frequency 2.20 MHz, output sampling frequency 469 kHz, data size 4 K (complex), Hanning window.

4. Basic parameters and its limitation

Analog-to-digital converter

The analog input bandwidth of the alone ADC is 400 MHz. Because unlike the receiver 50Ω single ended input, the input impedance of ADC is 1 kΩ and the input is differential, the matching and balancing RF transformers (Mini-Circuits) are used. These transformers unfortunately, limit the receiver analog input bandwidth from 0.3 MHz to 170 MHz range. The maximal sampling rate of both the ADC and DDC is 65 MHz. This limits the digital bandwidth of the receiver to 32.5 MHz. However, the undersampling (SuperNyquist mode) is possible.

The ADC dynamic range, related to the maximal Nyquist bandwidth, is 74 dB when we come out from the datasheet (2.2 MHz input). The related achievable maximal dynamic range is 149 dBFS/√Hz. From the first receiver measurement (Fig.2.) it is obvious that the practical maximal dynamic range of the receiver is better than 137 dBFS/√Hz. No analog input filter was used and thus the noise from the generator contributes to the measured noise (Fig. 2, 3.).

Digital down converter

The input data width of the AD6620 is 16 bits. This does not limit the dynamic range of the 14-bit ADC. The maximal decimation rate is 16384, the maximal dynamic range of DDC output is 120 dB. The practical maximal DDC output spectral width is limited by the processing power of the FIR to 1.3 MHz in the case of the parallel output. If the serial data output is used, the spectral width is limited to 1 MHz.

Digital signal processor

The maximal DSP input data rate is limited by the DMA to 4 MSPS (complex 16-bit) utilizable for the direct data acquisition from ADC. In the case of the serial transfer, the DSP limits the data rate to 625 KSPS. The external memory of DSP enables to use the data block size of 512 K sample. The DMA transfer (unlike the serial port) is restricted to internal memory, and the data rate of a big data block is thus limited by the speed of DSP which have to perform the data movement from internal to external memory and the page selection overhead.

The maximal data rate of the DSP output is related to the technique used. There is three possible connections: the RS 232 (2.8 KSPS), the DSP serial port (625 KSPS) and the Universal serial bus (250 KSPS).

5. Conclusion

A digital receiver using the new ADC is described. The promising parameters are suggested by the preliminary measurements (Fig.2, 3.). The system jitter performance is better than 4 ps (rms) when a built-in crystal oscillator is used. Further measurements will be presented at the conference.

Acknowledgement

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References

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[2] HALÁMEK, J. - JURÁK, P. – KASAL, M. – VILLA, M. – COFRANCESCO, P.: Analog-to-digital converter and dynamic range, J. Electrical engineering, 48 (1997), NO. 7-8, p. 183-189.